IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Atty Docket No. RA048DC3)

In the Application of:	Barth, et al.
Serial No:	Continuation of 09/561,868
Filed:	Herewith
Title:	PROTOCOL FOR COMMUNICATION WITH DYNAMIC MEMORY

Assistant Commissioner for Patents
Washington, DC 20231

PRELIMINARY AMENDMENT

Dear Sir:

Prior to the examination of the above-referenced application, kindly amend the application as follows:

IN THE SPECIFICATION:

(A version with markings to show changes made to the specification is attached herein as Exhibit A)

On page 1, line 2, please **insert** the following paragraph:

This application is a continuation of Application No. 09/561,868, filed on May 1, 2000 (pending); which is a continuation of Application No. 09/480,767, filed on January 10, 2000(pending); which is a continuation of Application No. 08/979,402 (now U.S. Patent 6,122,688), filed on November 26, 1997; which is a division of application No. 08/545,292 filed on October 19, 1995 (now U.S. Patent 5,748,914).

Please **substitute** the paragraph starting on page 16, line 19, with the following paragraph:

At step 814, the data is transmitted over the data bus (BusData[8:0]). During this step, the data may be transmitted to or from the target DRAM, depending on whether the data transfer operation is write or read operation. At some fixed period of time prior to the transmission of the last data packet, the controller transmits the terminate signal on the BusCtl line (step 816). Steps 816 and 814 are shown as a single step 812 to indicate that step 816 is performed during the performance of step 814.

Please **substitute** the paragraph starting on page 17, line 4, with the following paragraph:

As shall be explained below, one embodiment of the memory controller dynamically adjusts the interleave of data and control information to more fully utilize the channel. Interleave refers to the relative ordering of data, requests and control signals that are associated to multiple transactions. To allow dynamic

interleave adjustment, there is no fixed time period between the execution of steps 804 and 806. Rather, the controller is free to adjust the timing of step 806 relative to the timing of step 804 as needed to provide the desired interleave (e.g., to provide time to transmit the command control information for other transactions between execution of steps 804 and 806).

IN THE CLAIMS:

Kindly **cancel** claims 1-41 without prejudice.

Kindly **add** the following claims:

42. A method of operation in a semiconductor memory device, wherein the memory device receives an external clock signal and includes an array of memory cells, the method comprises:

receiving a first code synchronously with respect to the external clock signal, wherein the first code specifies that a write operation is to be initiated in the memory device

receiving a second code synchronously with respect to the external clock signal, wherein the second code specifies that a precharge operation is to be initiated automatically after initiation of the write operation;

detecting an external strobe signal, wherein the external strobe signal indicates when to begin sampling data;

sampling the data upon detection of the external strobe signal, wherein during the write operation, the memory device writes the data to the array; and

initiating the precharge operation automatically after the write operation is initiated.

43. The method of claim 42 wherein a first portion of the data is sampled synchronously with respect to the external clock signal.

44. The method of claim 43 further comprising sampling a second portion of data synchronously with respect to the external clock signal, wherein the first portion of data is sampled during an odd phase of the external clock signal, and the second portion

of data is sampled during an even phase of the external clock signal.

45. The method of claim 44 wherein the first and second portions of data are both sampled during the same clock cycle of the external clock signal.

46. The method of claim 42 wherein the precharge operation is initiated after the memory device writes the data to the array.

47. The method of claim 42 wherein the external strobe signal is detected by sampling from an external signal line synchronously with respect to the external clock signal.

48. The method of claim 42 further comprising receiving address information synchronously with respect to the external clock signal.

49. The method of claim 48, wherein the address information and the data are received from a common set of external signal lines.

50. The method of claim 49 wherein the first code, second code and address information are included in a write request packet.

51. The method of claim 42 further comprising:

receiving a third code synchronously with respect to the

external clock signal, wherein the third code specifies that the memory device initiate a sense operation;

initiating the sense operation; and

activating a row of sense amplifiers during the sense operation.

52. A method of controlling a semiconductor memory device, wherein the memory device includes an array of memory cells, the method comprises:

providing a plurality of control codes to the memory device wherein the plurality of control codes include a first code which specifies that a write operation be initiated in the memory device and a second code which specifies that a precharge operation be initiated automatically after initiation of the write operation;

delaying for an amount of time after providing the plurality of control codes; and

issuing an external strobe signal to the memory device after delaying for the amount of time, to signal the memory device to sample data, wherein the data is to be written to the array during the write operation.

53. The method of claim 52 further comprising issuing a first portion of the data and a second portion of the data to the memory device, wherein the first portion of the data is sampled during an odd phase of an external clock signal, and the second portion of the data is sampled during an even phase of the external clock signal.

54. The method of claim 53 wherein the first and second portions of the data are both issued during a first clock cycle of the external clock signal.

55. The method of claim 52 further comprising:

issuing additional portions of the data to the memory device; and

issuing the external strobe signal to the memory device to signal the memory device to stop sampling data.

56. The method of claim 52 further comprising providing address information to the memory device.

57. The method of claim 56 wherein the plurality of control codes and the address information are both included in a first packet.

58. The method of claim 57 wherein the data is included in a second packet and wherein the first packet and the second packet are transported over a common set of external signal lines.

59. The method of claim 52 wherein the plurality of control codes includes a third code which specifies that a row of sense amplifiers be activated.

60. A synchronous semiconductor memory device having an array which includes a plurality of memory cells, wherein the memory device receives an external clock signal, the memory device comprises:

a first input receiver to receive a first code synchronously with respect to the external clock signal, wherein, when the first code specifies a write operation, the memory device samples data upon detection of an external strobe signal;

a row of sense amplifiers coupled to the array, to store the data in the array during the write operation; and

a second input receiver to receive a second code synchronously with respect to the external clock signal, wherein the second code specifies that precharging the row of sense amplifiers occur automatically after the data is stored in the array.

61. The memory device of claim 60 further comprising a clock generator circuit to receive the external clock signal, wherein the data is sampled synchronously with respect to the external clock signal.

62. The memory device of claim 60 further comprising a plurality of input receiver circuits to sample a first portion of the data and a second portion of the data, wherein the first portion of the data is sampled during an odd phase of an external clock signal, and the second portion of the data is sampled during an even phase of the external clock signal.

63. The memory device of claim 62 wherein the first input receiver and the second input receiver are both included among the plurality of input receiver circuits.

64. The memory device of claim 62 wherein the plurality of input receiver circuits sample additional portions of data until detection of an external termination signal.

65. The memory device of claim 60 wherein the second input receiver samples address information synchronously with respect to the external clock signal.

66. The memory device of claim 60 further comprising a third input receiver to sample the external strobe signal.

67. The memory device of claim 60 wherein the first code and the second code are included in a packet.

68. The memory device of claim 60 further including a third input receiver to receive a third code synchronously with respect to the external clock signal, wherein the third code specifies that the row of sense amplifiers sense the contents of a row of memory cells included in the array.

69. The memory device of claim 68 wherein the data is stored in the row of memory cells included in the array during the write operation.

70. A dynamic random access memory device which receives an external clock signal, the memory device comprises:

an array of memory cells;

a first input receiver to receive a first code synchronously with respect to the external clock signal, wherein the first code indicates that a write operation be initiated in the memory device;

a second input receiver to receive an external strobe signal, wherein receipt of the external strobe signal indicates when the memory device is to begin sampling data, wherein the data is to be stored in the array during the write operation; and

a third input receiver to receive a second code which specifies that a row of sense amplifiers be precharged automatically after the data is stored in the array, wherein the second code is received synchronously with respect to the external clock signal.

71. The memory device of claim 70 further comprising a fourth input receiver to receive a third code synchronously with respect to the external clock signal, wherein the third code indicates that the row of sense amplifiers sense the contents of a row of memory cells of the array.

72. The memory device of claim 71 wherein further comprising a plurality of input receivers to receive address information which identifies the row of memory cells, wherein the address information is received synchronously with respect to the external clock

signal.

73. The memory device of claim 70 wherein the third input receiver also receives address information synchronously with respect to the external clock signal.

74. The memory device of claim 70 further comprising a plurality of input receiver circuits to sample a first portion of the data and a second portion of the data, wherein the first portion of the data is sampled during an odd phase of an external clock signal, and the second portion of the data is sampled during an even phase of the external clock signal.

75. The memory device of claim 74 wherein the first and second portions of the data are both sampled during a common clock cycle of the external clock signal.

76. The memory device of claim 70 wherein the first and second codes are included in a packet.

77. The memory device of claim 76 wherein the first and second codes are both included in a first packet and the data is included in a second packet.

78. The memory device of claim 77 wherein the first and second packet are multiplexed over a common set of external signal lines.

REMARKS

This Preliminary Amendment seeks to place this application in condition for allowance. In This application, Applicants present new claims which set forth novel and unobvious features of Applicants' invention.

Amendments to the Specification and Claim for Priority

Applicants have amended the specification to identify the continuation or related U.S. application data. Applicants claim priority to Application Serial No. 08/545,292 filed October 19, 1995, now U.S. Patent No. 5,748,914. Applicants claim such priority through Application No. 09/561,868, filed on May 1, 2000 (pending), which is a continuation of Application No. 09/480,767, filed on January 10, 2000; which is a continuation of Application No. 08/979,402 (now U.S. Patent 6,122,688), filed on November 26, 1997; which is a division of application No. 08/545,292 filed on October 19, 1995(now U.S. Patent 5,748,914). Accordingly, Applicants claim the benefit of the filing date of Application Serial No. 08/545,292 -- i.e., October 19, 1995. No new matter has been added.

In addition, Applicants have amended the specification to correct spelling and typographical errors. No new matter has been added.

Amendments to the Claims

Applicants submit new claims 43-78. No new matter has been added. The new claims are fully supported by the original specification. Examples of support for new claims 43-67 may be found in the original specification at page 13, line 10-16, page 14

lines 9-18; page 15, line 4 to page 16, line 20; page 19, lines 12-18; page 22, line 17 to page 23, line 2; and Figures 6, 8, 9, 12 and 13.

CONCLUSION

Applicants request entry of the foregoing amendment prior to examination of this application. Applicants submit that all of the claims present patentable subject matter which definitely set forth the novel and unobvious features of the invention. Accordingly, Applicants respectfully request allowance of all of the claims.

Respectfully submitted,

Date: May 25, 2001

Neil A. Steinberg
Reg. No. 34,735
650-947-5325

Exhibit A

(Version With Markings to show Changes Made to the Specification)

Starting on page 16, line 19:

At step 814, the data is transmitted over the data bus (BusData[8:0]). During this step, the data may be transmitted to or from the target DRAM, depending on whether the data transfer operation is write or read operation. At some fixed period of time prior to the transmission of the last [the last] data packet, the controller transmits the terminate signal on the BusCtl line (step 816). Steps 816 and 814 are shown as a single step 812 to indicate that step 816 is performed during the performance of step 814.

Starting on page 17, line 4:

As shall be explained below, one embodiment of the memory controller dynamically adjusts the interleave of data and control information to more fully utilize the channel. Interleave refers to the relative ordering of data, requests and control signals that are associated [assoicated] to multiple transactions. To allow dynamic interleave adjustment, there is no fixed time period between the execution of steps 804 and 806. Rather, the controller is free to adjust the timing of step 806 relative to the timing of step 804 as needed to provide the desired interleave (e.g., to provide time to transmit the command control information for other transactions between execution of steps 804 and 806).

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Atty Docket No. RA048DC3)

In the Application of:	)	
	)	
Barth, et al.	)	**Group:**
	)	
Serial No: Continuation of 08/561,868	)	
	)	**Before**
Filed: Herewith	)	**Examiner:**
	)	
Title: PROTOCOL FOR COMMUNICATION WITH DYNAMIC MEMORY	)	

Assistant Commissioner for Patents
Washington, DC 20231

REQUEST TO APPROVE DRAWING CHANGES

Dear Sir:

Applicants seek to amend Figure 19 to correct for an error. Attached is a photocopy of Figure 19 indicating the proposed change in red ink. No new matter has been added.

Further, Applicants seek to amend Figures 20A and 20B to remove extraneous matter. Attached is a photocopy of Figures 20A and 20B indicating the proposed change in red ink. No new matter has been added.

Applicants respectfully request approval of the proposed changes to Figures 19, 20A and 20B.

Respectfully submitted,

Date: May 25, 2001

Neil A. Steinberg
Reg. No. 34,735
650-947-5325

OPEN	CLOSE	~~PREVIOUS~~ CURRENT BANK STATE	NEW BANK STATE	ACTION
0	0	CLOSED	CLOSED	ILLEGAL
0	1	CLOSED	CLOSED	NO ACTION
1	0	CLOSED	OPEN	SENSE-CARD
1	1	CLOSED	CLOSED	SENSE-COMMAND-PRECHARGE
0	0	OPEN	OPEN	COMMAND
0	1	OPEN	CLOSED	COMMAND-PRECHARGE
1	0	OPEN	OPEN	PRECHARGE-SENSE-COMMAND
1	1	OPEN	CLOSED	PRECHARGE-SENSE-COMMAND-PRECHARGE

Figure 19

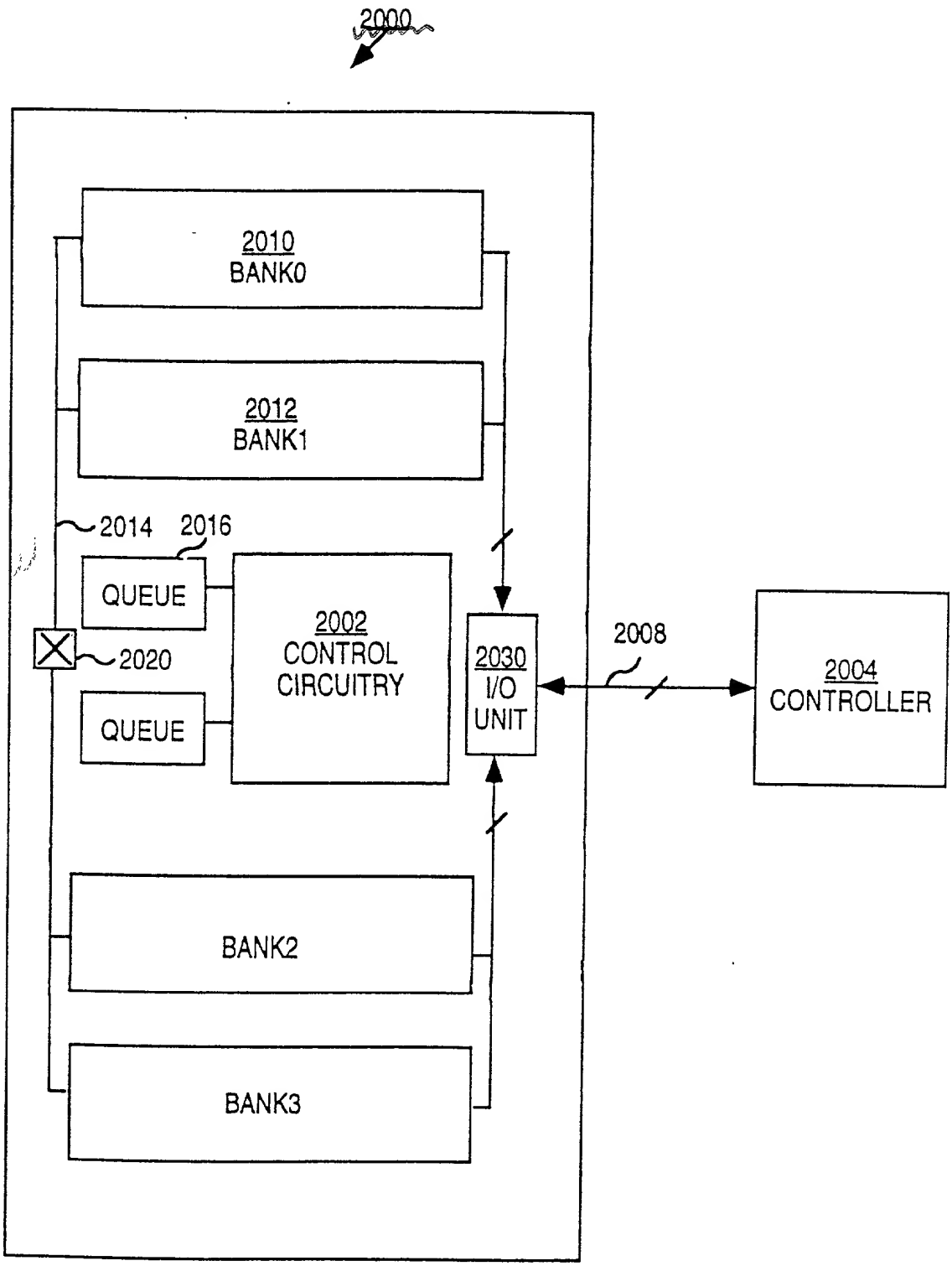
2000
2010
BANK0
2012
BANK1
2014
2016
QUEUE
2020
QUEUE
2002
CONTROL
CIRCUITRY
2030
I/O
UNIT
2008
2004
CONTROLLER
BANK2
BANK3

Figure 20A

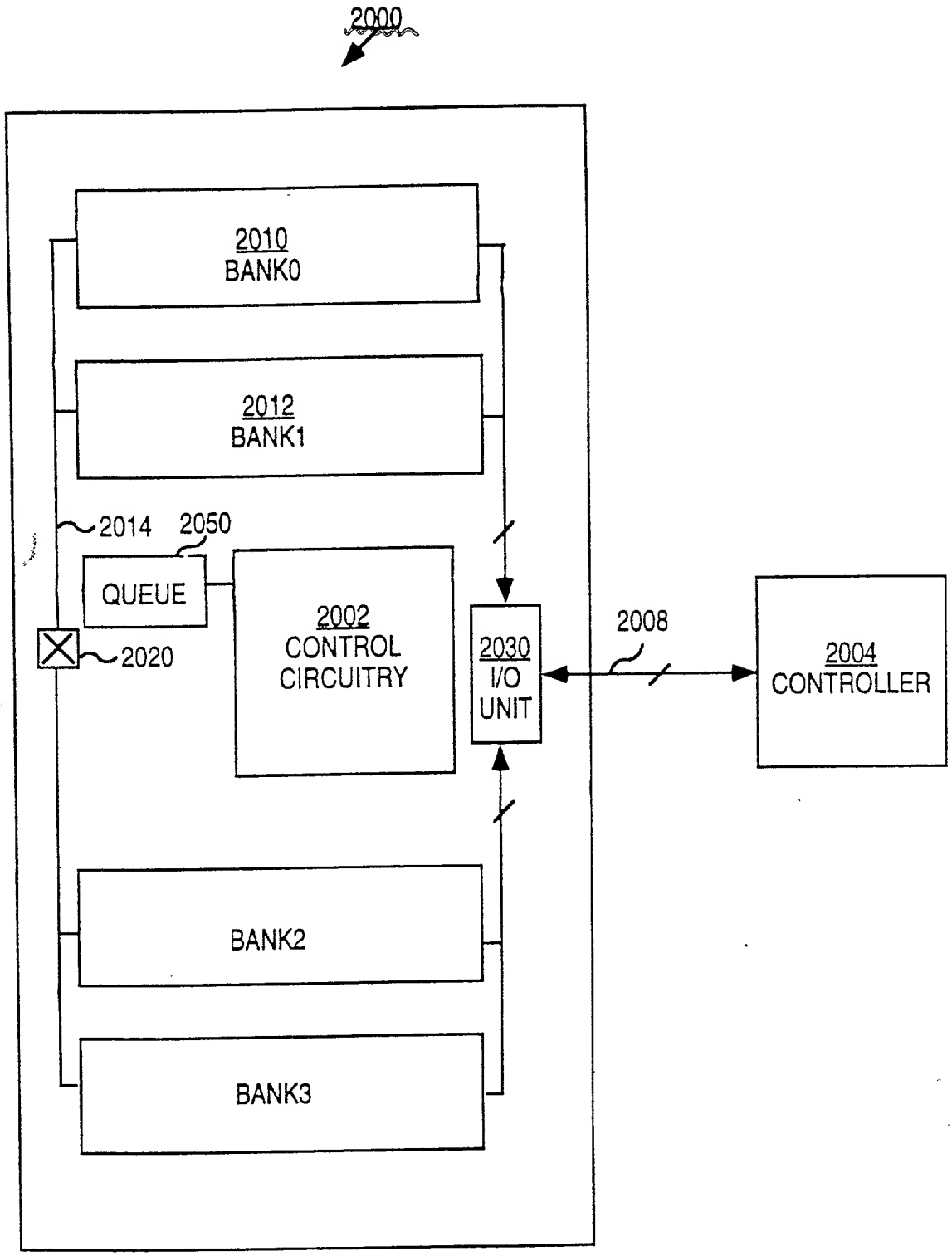
2000
2010
BANK0
2012
BANK1
2014
2050
QUEUE
2020
2002
CONTROL
CIRCUITRY
2030
I/O
UNIT
2008
2004
CONTROLLER
BANK2
BANK3

Figure 20B